REMARKS

Request for Continued Examination

Applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

Claims 1-3, 5-11, 13, 15-17, 19-21 are rejected under 35 USC 103a as being unpatentable over Kaiser et al. (US Patent #5,784,710) in view of Hasbun (US Patent #6,205,458)

Applicant asserts that claims 1-3, 5-11, 13, 15-17, 19-21 should not be rejected under 35 USC 103a as being unpatentable over Kaiser et al. in view of Hasbun because there is no motivation for a person skilled in the art to combine the teachings of Kaiser et al. with those of Hasbun to result in the present invention without further inventive process. In particular, applicant asserts that a combination of Kaiser et al. with Hasbun would at least fail to include the following limitations from claim 1 of the present invention:

> "selectively outputting the first logic address data or a second logic address data as a physical address data by using an address translator according to a control signal;
> turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data when it is required to protect the memory section from being accessed;" (claim 1 – emphasis added)

In the present invention, when it is required to protect the memory section from being accessed, a single control signal is utilized to control the address translator so that the second logic address data is outputted as the physical address data. In this way, the address translator selectively outputs either the first logic address data or the second logic address data as the physical address data according to the control signal. This operation is clearly claimed in claim 1, and is supported in paragraph [0036] of the present invention in reference to Figure 3. In particular, paragraph [0036] states, "if the controller generates the enable signal, the multiplexer 58 outputs physical address data that is different from

the first logic address data, and if the controller generates the disable signal, the multiplexer 58 outputs physical address data that is the same as the first logic address data. In other words, when the controller generates the enable signal, the address translator 50 translates the first logic address data generated by the microprocessor 40". By enabling (turning on) the address translator 50, the boot memory 62 is protected. This is supported in paragraph [037] stating, "Therefore, the data in the boot code section 62 is safe from being accessed, deleted, or updated incorrectly when the address translator 50 is turned on."

In contrast to this claimed operation of the present invention, the cited references of Kaiser et al. and Hasbun do not teach translating address data according to a control signal and turning on the address translator according to the same control signal to thereby protect the boot code section from being accessed. Additionally, applicant further asserts there is no motivation provided by the cited references to suggest such an operation.

Firstly, Kaiser et al. teaches performing address translation according to a control signal being the SELECT signal to multiplexer 205 in Figure 2. The teachings of Kaiser et al. concerning the SELECT signal are stated in column 4, lines 9-21, and state that if the N-bit address produced as the output of the concatenating circuit 203 matches a target address range, "then the SELECT line coupled to multiplexor circuit 205 will select the 1 input, which receives the resulting output of OR circuit 202. If there is not a hit, then the N-M upper bits of the address from the processor provided to the 0 input into multiplexor circuit 205 will be outputted as the N-M upper bits of a new address." In this way, even if a processor is not capable of addressing Initial Program Load (IPL) code, then the circuit of Kaiser et al. effectively translates the received address from the processor into an address capable of accessing this IPL code only if the target memory range is being accessed by the processor. (see col 4, lines 28-36) Therefore, processors can access IPL code being at addresses located above the address space of the processor, which is the goal of Kaiser et al. (See Abstract of Kaiser et al.)

However, Hasbun teaches a very different structure having a very different goal. For example, in col 6, lines 31-51, Hasbun teaches that a "block selector is toggled to swap physical address references between the first portion and a second portion (block) of the nonvolatile memory". The block selector can also be locked and thereby also prevents inadvertent updating of the currently selected boot block. In this way, the processor can

still be re-booted by accessing (i.e., reading) the boot code stored in the selected boot portion (block) of the nonvolatile memory as indicated by the block selector. (See col 4, lines 41-44 and Figure 6.) That is, the block selector itself acts as the control signal to prevent from being updated either the first or the second portion of the nonvolatile memory. The boot selector protects one of the portions from being updated by indicating the other portion for use when updating by the processor. Applicant notes that in order to boot, the processor still needs access to boot code stored in the selected section (ie, stored in the protected section).

Therefore, applicant firstly asserts that combining the teachings of Kaiser et al. with Hasbun would not result in the present invention as claimed in claim 1 because the SELECT signal utilized to translate the address for a processor not having enough bits needed to access IPL code on boot-up would not be the same as the boot selector signal which would need to select which block in the volatile memory needs to be accessed in order for the processor to boot. The reason these two control signals need to be different is that Hasbun teaches selecting a particular boot code section in the non-volatile memory according to the block selector, which would need to be selected separately than the SELECT signal used to turn on the address translator if the output of the concatenating circuit 203 matches a target address range as taught by Kaiser et al. Simply put, a person skilled in the art would be motivated to use separate control signals in order to gain the benefit as taught by Hasbun of having two exclusively selectable boot code (sections 342 or 344 in Figure 3 by Hasbun) that could be accessed with processors (units 108 or 109 in Figure 1 of Kaiser et al.) as taught by Kaiser et al. In order to maintain the principle of operation of the two cited references, the combination would require two independent control signals that are not the same. This is clearly different from the present invention as claimed in claim 1 because a single control signal is claimed in the present invention to turn on the address translator when it is required to protect the memory section from being accessed.

Secondly, applicant asserts that combining the teachings of Kaiser et al. with Hasbun would not result in the present invention as claimed in claim 1 because Hasbun does not teach preventing turning on the address translator "when it is required to protect the memory section from being accessed" (claim 1 of the present invention – emphasis added). As explained above, Hasbun instead simply teaches preventing updates to a

particular block but still allowing read access. In particular, refer to Figure 6 of Hasbun showing that no matter what the setting of the "Block Selector" bit, both blocks 1 and 2 of the non-volatile memory are still accessible. Specifically, when the block selector is 1, boot occurs from block 1 and updates are permitted to block 2. Alternatively, when the block selector is 0, boot occurs from block 2 and updates are permitted to block 1. Applicant notes that read access must be enabled for boot to occur and therefore the teachings of Hasbun are not equivalent to the present invention of "turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data when it is required to protect the memory section from being accessed" (claim 1 – emphasis added)

For at least the above-described reasons, applicant asserts that claim 1 should not be found unpatentable over the teachings of Kaiser et al. in view of Hasbun. Similar arguments also apply to independent claim 7, and the dependent claims should be found allowable for at least the same reasons. Reconsideration of claims 1-21 is respectively requested. Further comments regarding the patentability of specific dependent claims is provided below.

Regarding claims 15, 16 and 19, 20, in addition to the above provided arguments for the base claims, applicant points out that that neither Kaiser et al. nor Hasbun et al. teach protecting boot code for the microprocessor from being accessed. Instead, as explained above, both Kaiser et al. and Hasbun teach allowing at least read access to the boot code for the microprocessor at all times. For at least this reason, claims 15, 16, 19, and 20 should be found allowable with respect to the cited references. Reconsideration of claims 15, 16, 19, and 20 is respectively requested. Claims 17 and 21 are dependent claims and should therefore also be allowable for at least the same reasons.

Claims 4, 12, 14, and 18 are rejected under 35 USC 103a as being unpatentable over the combination of Kaiser et al. (US Patent %,784,710) and Hasbun *US Patent #6,205,458) references as applied above, and further in view of Debruler (US Patent #4,539,637).

As previously mentioned, claims 4, 12, 14, and 18 are dependent upon claims 1 and 7 believed to be allowable by the applicant for the above-stated reasons. Therefore claims 4, 12, 14, and 18 should be found allowable for at least the same reasons.

New Claim

New independent claim 22 is added being similar to previously presented claim 1. The differences between claim 1 and claim 22 lie in the preamble and the inclusion of the step: "protecting the memory section from being accessed by outputting the second logic address data as the physical address data from the address translator when it is required to protect the memory section from being accessed". No new matter is entered. For example, such operation is taught in paragraph [0063] in reference to Figure 3 of the original specification as filed.

Concerning the patentability of new claim 22 with respect to the cited references of Kaiser et al. and Hasbun, applicant points out that neither references teach, either alone or in combination, the above step in relation to the other steps of claim 22. In particular, Kaiser et al. teach checking for a match (output of the OR circuit 202) to control what will be outputted on the N-M upper bits of the new address. In this way, access to the IPL code is effectively allowed for processors having lower address bit numbers. See Kaiser et al. in col. 4, lines 32-34 stating, "... then circuitry 20 will effectively translate the received address from the processor into an address capable of accessing this IPL code." Applicant notes that allowing access to an IPL memory section is not equal or similar to "protecting the memory section from being accessed by outputting the second logic address data as the physical address data from the address translator when it is required to protect the memory section from being accessed". Additionally, as explained above, Hasbun does not protect any memory section from being accessed because both boot code sections can be accessed (either read or update access) at all times. In particular, see refer to Figure 6 of Hasbun showing that no matter what the setting of the "Block Selector" bit, both blocks 1 and 2 of the non-volatile memory are still accessible.

For at least these reasons, applicant asserts that new claim 22 should be found allowable with respect to the cited references. Consideration of new claim 22 is respectfully requested.

Sincerely yours,

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